DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with **Mark Gleason** on **05/20/2009**.

The application has been amended as follows:

Claims 28-35 are canceled.

Allowable Subject Matter

2. Claims 11, 14-25, 27, and 37-39 are allowed over the prior art of record.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

The prior art of record neither teach nor render obvious the instant application claimed invention as a whole, in particular, the prior art fails to teach "a wiring block made of plastic with contact pads on its outer sides and with lines comprising nanoparticles with carbonized short-circuit paths between the nanoparticles in its volume." as recited in claims 11, " anisotropically oriented nanoparticles in its volume, the lines electrically connecting the contact pads on the outer sides to one another according to a circuit layout, the first component and the second component being

arranged on different non-opposite outer sides of the wiring block and the connections being connected to the contact pads" recited in claim 14, "wherein the lines comprise carbonized plastic, the lines including nanoparticles with carbonized short-circuit paths between the nanoparticles, wherein the lines comprise anisotropically oriented nanoparticles." as recited in claim 15, " nanoparticles with carbonized short-circuit paths between the nanoparticles in its volume, the lines electrically connecting the contact pads on the outer sides to one another according to a defined circuit layout, the first component and the second component being arranged on different outer sides of the wiring block and the connections being connected to the contact pads", as recited in claim 16, "anisotropically oriented nanoparticles in its volume, wherein the wiring block includes a plastic volume through which the lines extend, and includes at least six outer sides configured for population with electronic devices or components, such that line routing through the wiring block is configurable for three-dimensional wiring between contact pads", as recited in claim 27, "a wiring block made of plastic with nanoparticles and having contact pads on the outer sides and with lines in its volume", as recited in claim 37.

Claims 14-25, 27, and 37-39 are also allowed as being directly or indirectly dependent of the allowed base claims 11, 14, 15, 16, 27 and 37.

Relevant Art

4. Baker et al. (US5, 869,896 A) teaches an electronic module includes multiple stacked bare IC chips ("a stack") and a sensor assembly that is mechanically coupled to

an end surface of the stack. Electrical connection between the sensor assembly and the stack is provided by a metallization layer disposed on a side-surface of the stack. Specifically, wiring of the sensor assembly extends to an edge surface thereof corresponding to the side-surface of the stack where it electrically connects to the side-surface wiring. The IC chips of the stack are similarly electrically connected to the side-surface wiring. Multiple sensors (e.g., CCD arrays) may be electrically and mechanically coupled to multiple surfaces of the stack for providing a, e.g., multi-view imaging module. Multiple electrical and mechanical options exist for the connection of sensors to stacks within electronic modules.

Ross (US 6,222,737) teaches A chip module comprising a chip array which includes an interconnect substrate having opposed, generally planar surfaces and a first interconnect pad array disposed on at least one of the surfaces thereof. Attached to the interconnect substrate is at least one integrated circuit chip of the chip array which is electrically connected to the first interconnect pad array. The chip module further comprises a package which itself comprises a main body defining a cavity sized and configured to receive the chip array and having a generally planar interconnect shelf which extends within the cavity and includes a second interconnect pad array disposed thereon. The package also includes a lid which is attachable to the main body. The chip array is insertable into the cavity such that the first and second interconnect pad arrays are in aligned contact with each other and the attachment of the lid to the main body encloses and seals the chip array within the package.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andargie M. Aychillhum whose telephone number is (571) 270-1607. The examiner can normally be reached on (Mon-Fri from 8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
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/Dean A. Reichard/
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A.A.
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